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Inventor(s): Lee et al.

Serial No.: 10/608,606

Examiner: Crane, Sara W

Filing Date: June 27, 2003

Group Art Unit: 2249

Title: METHOD FOR FABRICATING A PACKAGING DEVICE FOR SEMICONDUCTOR DIE
AND SEMICONDUCTOR DEVICE INCORPORATING SAME

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

- (a) ☒ Under 37 CFR 1.97(b).
(Within three months of filing national application; or date of entry of national application; or before mailing date of first Office action on the merits; whichever occurs last).
- (b) ☐ Under 37 CFR 1.97(c) together with *either* a:
☐ Statement under CFR 1.97(e), or
☐ \$180.00 fee under 37 CFR 1.17(p).
(After the CFR 1.97(b) time period, but before a final action or notice of allowance, whichever occurs first).
- (c) ☐ Under 37 CFR 1.97(d) together with: a
Statement under 37 CFR 1.97(e), *and*
\$180.00 fee as set forth in 37 CFR 1.17(p).
(After a final action or notice of allowance, whichever occurs first, but before payment of the issue fee).

☐ STATEMENT UNDER 37 CFR 1.97(e)

The undersigned certifies that:

- ☐ Each item of information contained in the Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the statement, or
- ☐ No item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned after making reasonable inquiry, was known to any individual designated in 37 CFR § 1.56(c) more than three months prior to the filing of the Information Disclosure Statement.

☐ PRIOR APPLICATIONS

References identified with an asterisk (*) in the enclosed PTO Form 1449, were disclosed in prior Patent Application No. , filed , now U.S. Patent No. , and, as such, copies thereof are not included pursuant to the provisions of 37 CFR 1.98(d).

☐ FOREIGN LANGUAGE DOCUMENTS

A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO form 1449, as presently understood by the individual(s) designated in 37 CFR 1.56(c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

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☒ **FEE AUTHORIZATION**

Please charge to Deposit Account **50-3718** the sum of \$0.00. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **50-3718** pursuant to 37 CFR 1.25.

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Date of Facsimile: 11/7/06

Typed Name: Joy Reinhart

Signature: Joy Reinhart

Respectfully submitted,

Lee et al.

By Jay B. Malkin

Jay B. Malkin
Attorney/Agent for Applicant(s)

Reg. No. 31,393

Date: 11/7/06

Telephone No. (303) 298-9888

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Form PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTORNEY DOCKET NO. 70030260-1	SERIAL NO. 10/608,606
	APPLICANT Lee et al.	
	FILING DATE June 27, 2003	GROUP 2249

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	*	DOCUMENT NUMBER	DATE	NAME
		5,640,048	June 17, 1997	Selna
		5,986,885	November 16, 1999	Wyland
		6,084,295	July 4, 2000	Horiuchi et al.
		6,191,477	February 20, 2001	Hashemi
		6,268,654	July 31, 2001	Glenn et al.
		6,620,720	September 16, 2003	Moyer et al.

FOREIGN PATENT DOCUMENT

		DOCUMENT NUMBER	DATE	NAME	TRANSLATION YES	NO

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

	Syd R. Wilson, Clarence J. Tracy, and John L. Freeman, Jr., "Handbook of Multilevel Metallization for Integrated Circuits", Noyes Publ., Westwood, New Jersey (1993), pp. 868 - 872.
	Electronic Packaging and Production, "Innovative PCB Reinforcement", (February, 1997), p. 1.
	Johannes Adam, "New Correlations Between Electrical Current and Temperature Rise in PCB Traces", Proc. 20th IEEE Semi-Therm Symp., (March 2004), pp. 1 - 8.

EXAMINER	DATE CONSIDERED
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* Copies of these references are not enclosed Pursuant to 37 CFR 1.98(d). (See accompanying IDS)

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